REMARKS

This is a full and timely response to the outstanding Action mailed June 17, 2004. Upon entry of the amendments in this response, claims 1 – 15 remain pending. In particular, Applicants have amended claims 1, 4 – 6, 9 and 12 - 14. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Objections to the Drawings

The Office Action objects to the drawings due to various informalities. Specifically, several reference characters used in the drawings were not mentioned in the specification and *vice versa*. In this regard, Applicants have provided replacement drawing sheets to be entered and has amended the specification as indicated above. Applicants respectfully assert that no new matter has been added. Specifically, Applicants have:

removed reference characters 250 and 270 in the amended Fig. 1;

replaced reference character 230 with reference character 320 such that the drawing is consistent with the description;

added reference character D11 to designate the diode in Fig. 1;

replaced reference character 21 with reference character 20 in the amended Fig. 2;

added reference character D1 to designate the diode formed with the anode being the P+ contact regions 32 and the cathode being the N-well 18;

removed reference characters 80, 82, 84, 86, 88, 90, 92, 94, 96, and 98 from Fig. 4 since these reference characters are not mentioned in description; and

replaced reference character 28 with reference character 38 in the amended Figs. 5D and 5E.

With respect to reference character 66 in Fig. 5, this reference character is mentioned in Line1 in the ninth paragraph of the DESCRIPTION OF THE PREFERRED EMBODIMENTS. Thus, Applicants respectfully assert that no amendment is necessitated.

In the Specification

The specification has been amended to designate the N well with reference character 180 and contacts with reference character 300 (*See* Page 2 Lines 7 and 17 of the specification). It is respectfully noted that reference character 36 is used to designate polysilicon (*See* Page 8 Lines 14 and 15 of the specification). No new matter has been added.

In addition, the Office Action indicates that the specification stands objected to as failing to provide proper antecedent basis for the claimed subject matter. Applicants respectfully traverse the objection. Specifically, in the first paragraph of the DESCRIPTION OF THE PREFERRED EMBODIMENTS, a first electrical conductor system is disclosed that is created to connect the P+ contact region 32 to a first voltage source, typically the active integrated circuit signal input pad 8, and a second electrical conductor system is created which connects NFET1 source 61 and NFET2 source 62 as well as the substrate P+ contacts 30 to a second voltage source, typically ground. In the ninth paragraph of the DESCRIPTION OF THE PREFERRED EMBODIMENTS, it is described that the conductor system 64 for the P+ contact region 32 and the conductor system 66 for the N+ NFET source elements 61 and 62 and the P+ substrate contacts 30 are created by a blanket evaporation of a metal, typically aluminum or aluminum doped with 1% silicon(See Line 1 to 3 in the paragraph). Thus, Applicants respectfully assert that proper antecedent basis for the subject matter of claims 13 and 14 has been provided.

Rejections Under 35 U.S.C. 112, Para. 2

The Office Action indicates that claims 1-15 stand rejected under 35 U.S.C. 112, Para. 2, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicant regards as the invention. As set forth above Applicants have amended the claims and respectfully assert that the rejection has been accommodated.

Rejections Under 35 U.S.C. 103(a)

The Office Action indicates that claims 3-7, 9, 12 and 15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of *Jun et al.* (U.S. Publication No. 2002/0084485) and *Floyd et al.* (U.S. Publication No. 2002/0055232). Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of *Jun et al*, *Floyd et al.* and *Sheu et al.*(U.S. Patent No. 5,998,832). Claim 8 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of *Jun et al.*, *Floyd et al.* and *Liau et al.* (U.S. Patent No. 5,783,850). Claim 10 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of *Jun et al.*, *Floyd et al.* and *Chang et al.* (U.S. Patent No. 5,814,547). Claim 11 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of *Jun et al., Floyd et al* and *Hau et al.* (U.S. Patent No. 6,475,875). Additionally, Claims 13 and 14 claims rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of *Jun et al.*, *Floyd et al.* and *Wolf Silicon Processing*. Applicants respectfully traverse the rejections under 35 U.S.C. 103(a) for at least the following reasons.

As set froth above, all the presently pending rejections under 35 U.S.C. 103 rely on the combination of Applicant's Prior Art in view of *Jun et al.* In this regard, Applicants respectfully

assert that the cited combination is improper and, therefore, the rejection is legally deficient. Specifically, as described in the fourth paragraph of the **DESCRIPTION OF PRIOR ART**, there is a large capacitance of approximately 0.27 pF associated with Applicant's Prior Art (See Lines 4 and 5). Thus, it is not suitable for a high frequency application. The main issue associated with Applicant's Prior Art is to reduce the ESD device capacitance. Those skilled in the art should have the motivation of reducing the ESD device capacitance instead of reducing the breakdown voltage. Therefore, it would not have been obvious to modify the semiconductor of Applicant's Prior Art to include the use of isolation elements as disclosed in *Jun*.

In addition, isolation elements as disclosed in *Jun* do not help reducing avalanche breakdown. As described in Paragraph [0015] in *Jun*, the object to reduce the avalanche breakdown voltage is achieved by providing a controllable dummy layer, which functions as an STI block **to remove the STI between the n+ and p+ regions of the diode**. Thus, even if one skilled in the art had the motivation to reduce the breakdown voltage, one would be motivated to remove the isolation elements rather than use them.

In contrast to Applicants' claims, the key point in *Jun* is to provide a controllable dummy layer, which functions as an STI block to remove the STI between the n+ and p+ regions of the diode. The isolation elements in *Jun* do not necessarily abut the doped regions. Thus, Applicants respectfully asserts that it would not have been obvious to modify the semiconductor of Applicant's Prior Art to include the use of isolation elements as disclosed in *Jun*. Therefore, Applicant respectfully assert that the combination is improper, thereby rendering the rejection defective, because a proper combination has not been cited for teaching or reasonably suggesting all of the features/limitations recited in Applicants' claims.

Turning now to the claims, claim 1 recites:

1. ***A low capacitance depletion mode SCR and NFET element integrated circuit semiconductor device structure with associated parasitic bipolar transistors on a substrate for the purpose of providing electrostatic voltage discharge protection to the active semiconductor devices***, comprising:

a first doped region of opposite dopant than said substrate;

a second doped region, of opposite dopant than said first doped region, within said first doped region;

a plurality of third doped regions within said substrate of opposite dopant than said substrate;

a gate element overlaying said substrate surface between a first element and second element of said third doped regions;

a gate element overlaying said substrate surface between a third element and fourth element of said third doped regions;

a first isolation element between said second element of said third doped region and a first side of said second doped region;

a second isolation element between said third element of said third doped region and a second side of said second doped region;

a plurality of fourth doped regions within said substrate of similar dopant as said substrate;

an electrical conductor system for said second doped region;

an electrical conductor system for said first and fourth elements of said third doped regions and for the first and second elements of said fourth doped regions; and

a surface passivation layer for said ESD protection device.

(*Emphasis Added*).

Applicants respectfully assert that the cited references, either individually or in proper combination, are legally deficient for the purpose of rendering obvious claim 1. Specifically, Applicants respectfully assert that the references do not teach or reasonably suggest at least the features/limitations emphasized above in claim 1. Therefore, Applicants respectfully assert that claim 1 is in condition for allowance. Since claims 2 - 15 are dependent claims that incorporate all the features/limitations of claim 1, Applicants respectfully assert these claims also are in condition for allowance. Additionally, these claims recite other features/limitations and combinations thereof that may serve as an independent basis for patentability.

With respect to the additionally articulated rejections of claims 2, 8, 10, 11, 13 and 14, Applicants respectfully assert that the rejections of these claims also are legally deficient. Specifically, none of these references teaches or reasonably suggests at least the features/limitations emphasized above in claim 1. Therefore, Applicants respectfully assert that these claims are in condition for allowance despite the additional rejections.

Cited Art Made of Record

The cited art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicants respectfully submit that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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In the Drawings

The attached sheets of drawings include changes to Fig. 1, Fig. 2, Fig. 4, Fig. 5D, and Fig. 5E. These sheets replace the original sheets.

Attachments

Tab A: Annotated drawing sheets

Tab B: Clean copy of drawing sheets

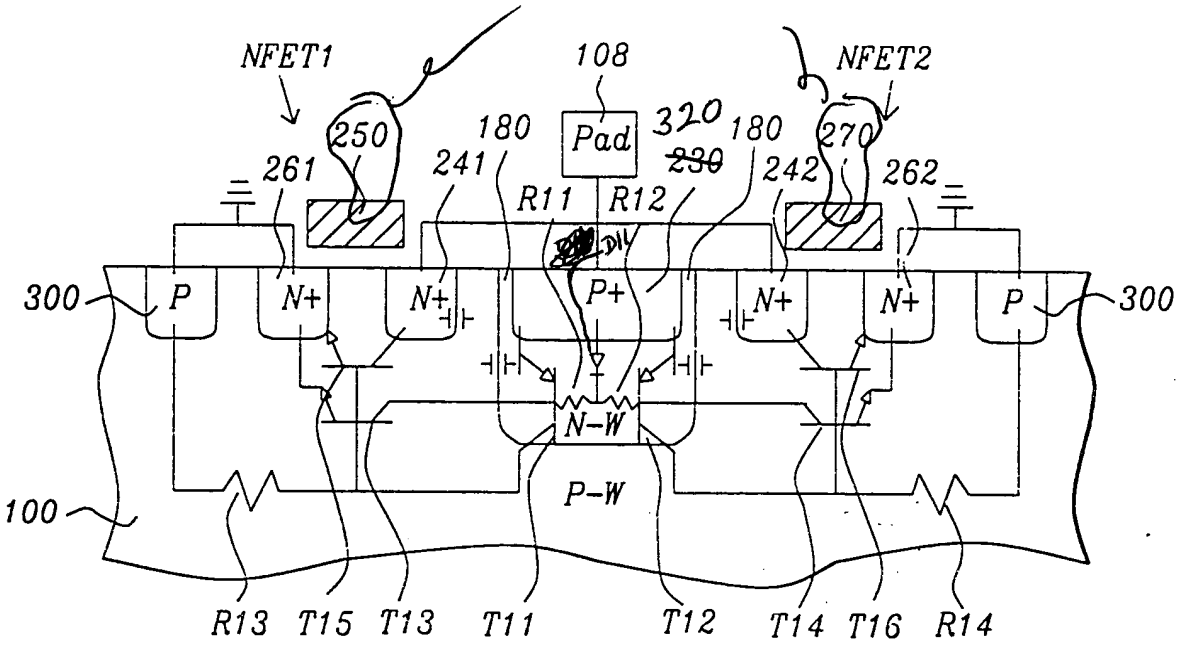

FIG. 1 – Prior Art

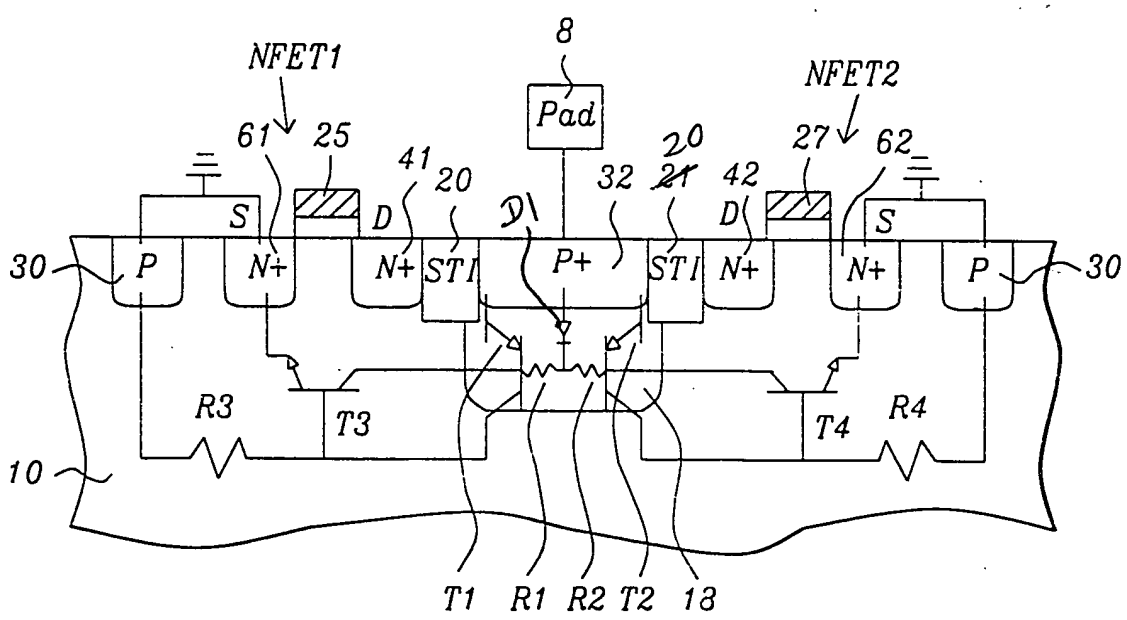

FIG. 2

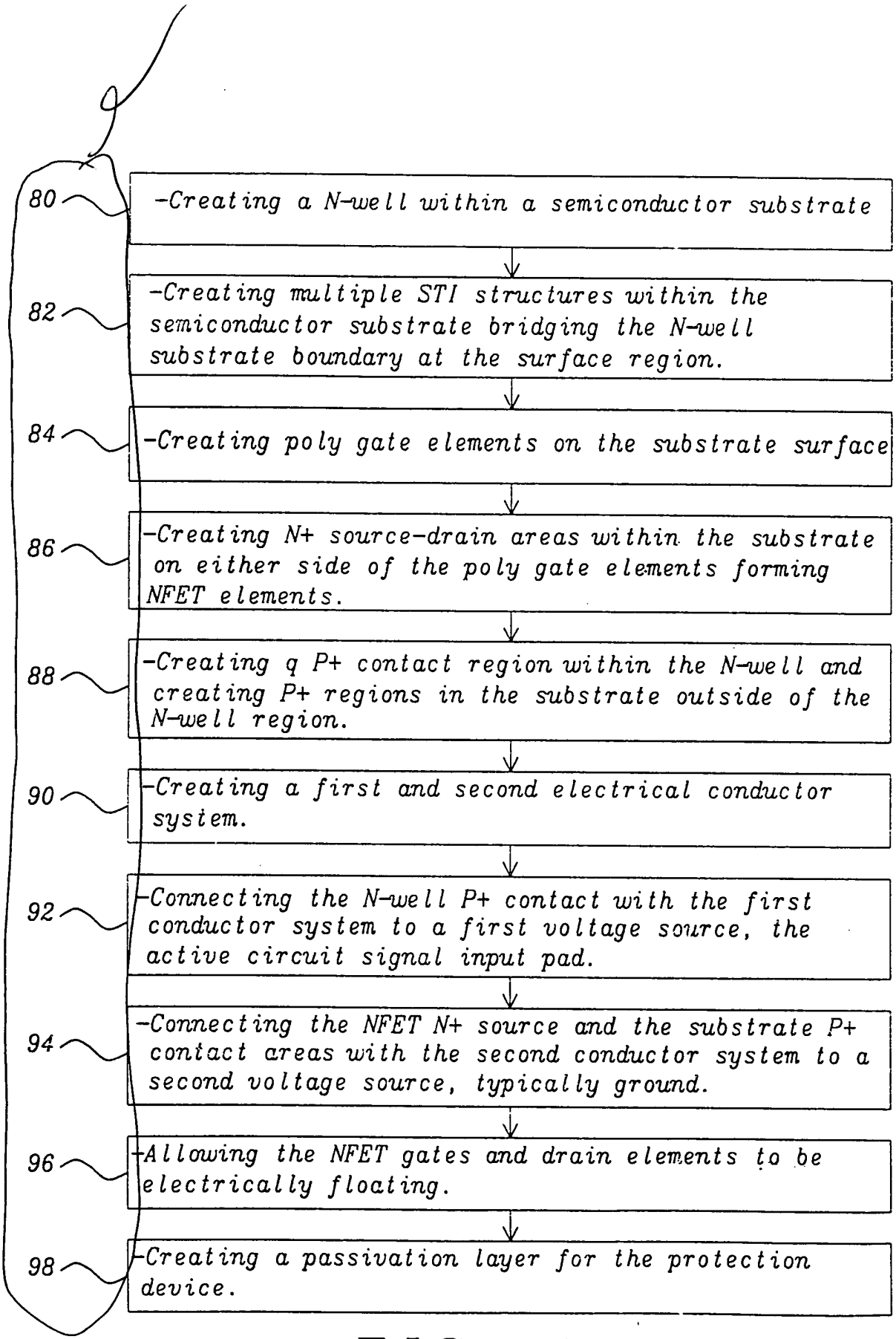
80
-Creating a N-well within a semiconductor substrate
82
-Creating multiple STI structures within the semiconductor substrate bridging the N-well substrate boundary at the surface region.
84
-Creating poly gate elements on the substrate surface
86
-Creating N+ source-drain areas within the substrate on either side of the poly gate elements forming NFET elements.
88
-Creating q P+ contact region within the N-well and creating P+ regions in the substrate outside of the N-well region.
90
-Creating a first and second electrical conductor system.
92
-Connecting the N-well P+ contact with the first conductor system to a first voltage source, the active circuit signal input pad.
94
-Connecting the NFET N+ source and the substrate P+ contact areas with the second conductor system to a second voltage source, typically ground.
96
-Allowing the NFET gates and drain elements to be electrically floating.
98
-Creating a passivation layer for the protection device.

FIG. 4

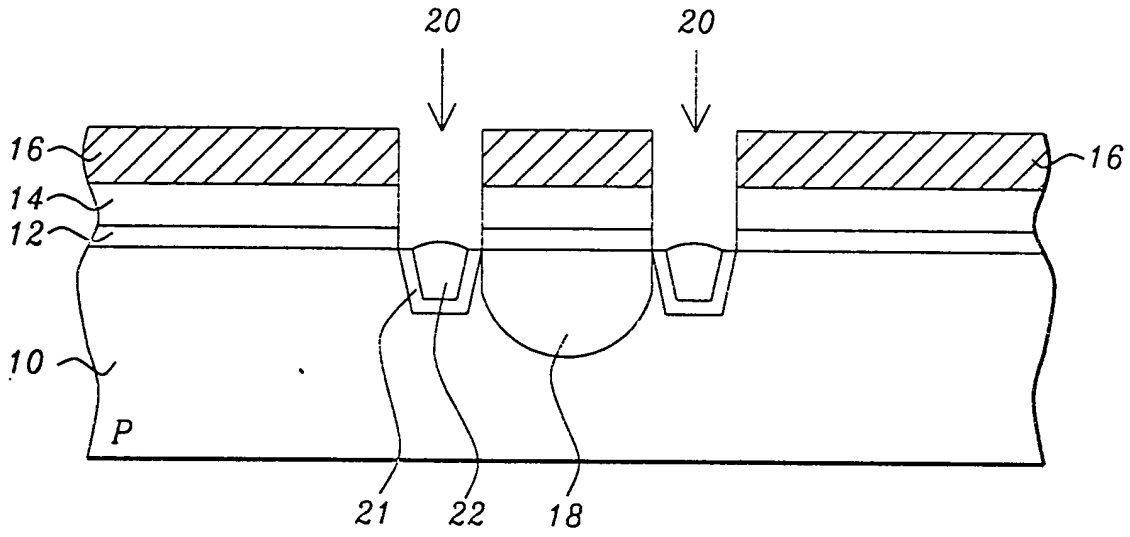
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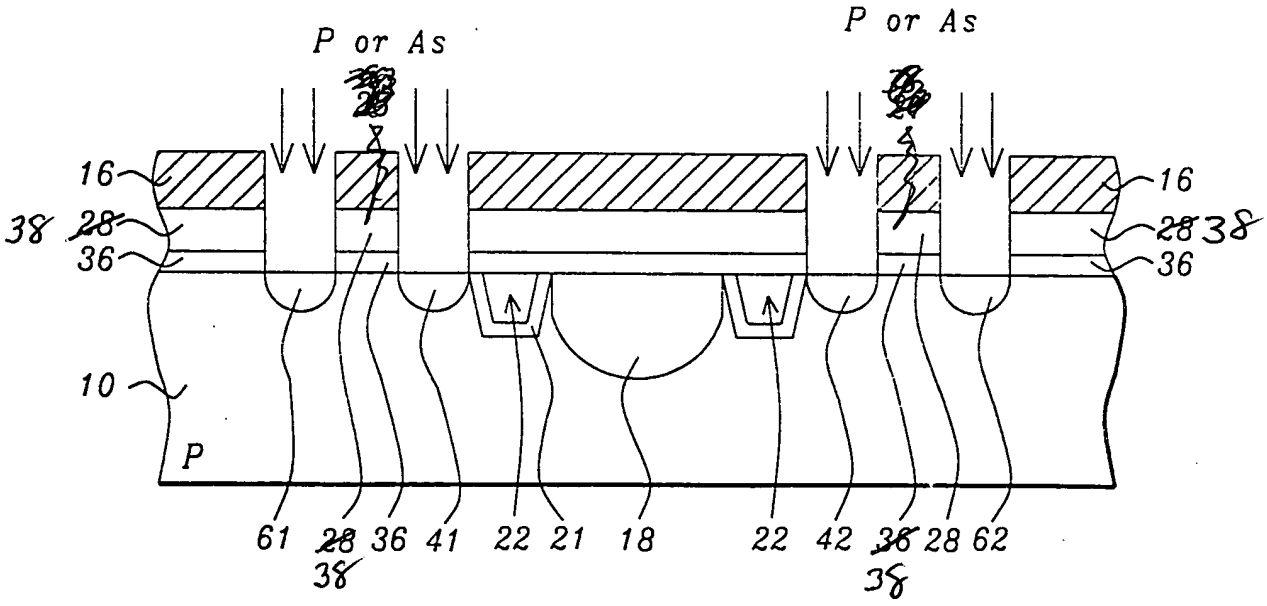
FIG. 5C


P or As
P or As
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36
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36
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FIG. 5D

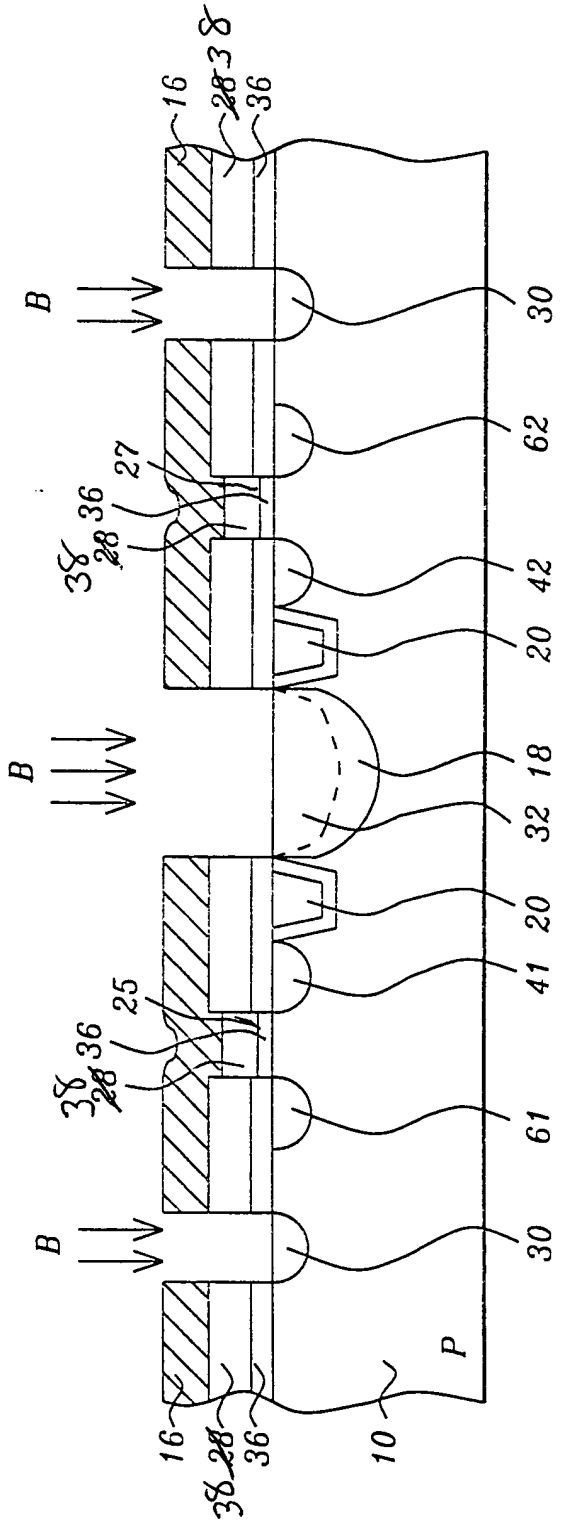
B
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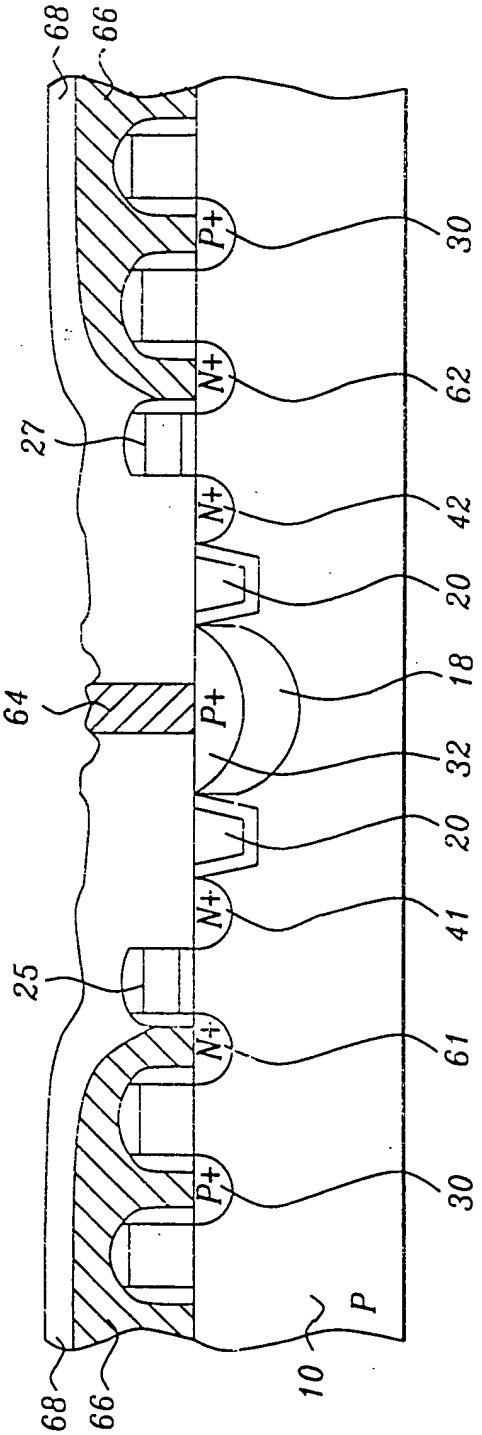
FIG. 5E


68
66
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64
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P+
N+
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61
10

FIG. 5F